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1 LISTING OF CLAIMS

2 We claim:

3 1. (currently amended) An apparatus comprising:

4 descriptor logic on a computer readable medium, said apparatus for controlling flow of data
5 between first and second data processing systems via a memory, said descriptor logic for
6 generating ~~in entirety~~ a plurality of descriptors including a frame descriptor defining a data
7 packet to be communicated between a location in the memory and the second data processing
8 system,

9 a pointer descriptor identifying the location in the memory; and

10 a descriptor table for storing ~~in physical entirety on the computer readable medium~~, the plurality
11 of descriptors generated by the descriptor logic for access by the first and second data processing
12 systems.

13 2. (previously presented) An apparatus as claimed in claim 1, wherein said apparatus employs
14 Logical Communication Port architecture, and the descriptor table is stored in one of the first
15 data processing system and the second data processing system.

16 3. (original) An apparatus as claimed in claim 1, wherein the descriptor table is stored in the
17 second data processing system.

18 4. (previously presented) An apparatus as claimed in claim 1, wherein said apparatus employs
19 Logical Communication Port architecture, and the descriptor logic generates a branch descriptor
20 comprising a link to another descriptor in the descriptor table.

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1 5. (original) An apparatus as claimed in claim 4, wherein the descriptor table comprises a
2 plurality of descriptor lists sequentially linked together via branch descriptors therein.

3 6. (original) An apparatus as claimed in claim 4, wherein the descriptor table comprises a cyclic
4 descriptor list.

5 7. (previously presented) An apparatus as claimed in claim 1, wherein said apparatus employs
6 Logical Communication Port architecture, and the first data processing system comprises a host
7 computer system.

8 8. (original) An apparatus as claimed in claim 1, wherein the second data processing system
9 comprises a data communications interface for communicating data between the host computer
10 system and a data communications network.

11 9. (currently amended) A data processing system processor comprising:

12 a host processing computer system having a memory, a data communications interface for
13 communicating data between the host computer system and a data communications network, and
14 apparatus comprising:

15 descriptor logic on a computer readable medium, said apparatus for controlling flow of data
16 between first and second data processing systems via a memory, said descriptor logic for
17 generating a plurality of descriptors including a frame descriptor defining a data packet to be
18 communicated between a location in the memory and the second data processing system, and

19 a pointer descriptor identifying the location in the memory; and

20 a descriptor table for storing on the computer readable medium, ~~in physical entirety~~ the plurality
21 of descriptors generated by the descriptor logic for access by the first and second data processing

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1 systems, for controlling flow of data between the memory of the host computer system and the
2 data communications interface.

3 10. (currently amended) A method comprising controlling flow of data between first and second
4 data processing systems via a memory, the step of controlling comprising:

5 by descriptor logic, generating in entirety a plurality of descriptors including a frame descriptor
6 defining a data packet to be communicated between a location in the memory and the second data
7 processing system,

8 a pointer descriptor identifying the location in the memory; and

9 storing the descriptors generated by the descriptor logic in a descriptor table for access by the
10 first and second data processing systems.

11 11. (original) A method as claimed in claim 10, comprising storing the descriptor table in the first
12 data processing system.

13 12. (original) A method as claimed in claim 10, comprising storing the descriptor table in the
14 second data processing system.

15 13. (original) A method as claimed in claim 10, comprising, by the descriptor logic, generating a
16 branch descriptor comprising a link to another descriptor in the descriptor table.

17 14. (original) A method as claimed in claim 13, comprising linking a plurality of descriptor lists
18 together in series via branch descriptors to form the descriptor table.

19 15. (original) A method as claimed in claim 10, wherein the first data processing system
20 comprises a host computer system.

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1 16. (original) A method as claimed of claim 10, wherein the second data processing system
2 comprises a data communications interface for communicating data between the host computer
3 system and a data communications network.

4 17. (currently amended) A computer program product comprising a computer ~~usable~~ readable
5 medium having computer readable program code means embodied therein for causing control of
6 flow of data between first and second data processing systems, the computer readable program
7 code means in said computer program product comprising ~~computer readable program code~~
8 ~~means~~ for causing a computer to effect the functions of claim 1.

9 18. (currently amended)) A computer program product comprising a computer ~~usable~~ readable
10 medium having computer readable program code means embodied therein for causing data
11 processing, the computer readable program code means in said computer program product
12 comprising ~~computer readable program code means~~ for causing a computer to effect the
13 functions of a data processing system comprising:

14 a host processing system having a memory, a data communications interface for communicating
15 data between the host computer system and a data communications network, and

16 apparatus comprising:

17 descriptor logic, said apparatus for controlling flow of data between first and second data
18 processing systems via a memory, said descriptor logic for generating a plurality of
19 descriptors including a frame descriptor defining a data packet to be communicated
20 between a location in the memory and the second data processing system, and

21 a pointer descriptor identifying the location in the memory; and

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1 a descriptor table for storing the descriptors generated by the descriptor logic for access
2 by the first and second data processing systems, for controlling flow of data between the
3 memory of the host computer system and the data communications interface.

4 19. currently amended) An article of manufacture comprising a computer ~~usable~~ readable
5 medium having computer readable program code means embodied therein for causing control of
6 flow of data between first and second data processing systems, the computer readable program
7 code means in said article of manufacture comprising ~~computer readable program code means for~~
8 causing a computer to effect the steps of a method ~~comprising~~ controlling flow of data between
9 first and second data processing systems via a memory, the step of controlling comprising:
10 by descriptor logic, generating a plurality of descriptors including a frame descriptor defining a
11 data packet to be communicated between a location in the memory and the second data
12 processing system,
13 a pointer descriptor identifying the location in the memory; and
14 storing the descriptors generated by the descriptor logic in a descriptor table for access by the
15 first and second data processing systems.

16 20. (currently amended) A program storage device readable by machine, tangibly embodying a
17 program of instructions executable by the machine to perform method steps for controlling flow
18 of data between first and second data processing systems, said method ~~steps comprising the steps~~
19 ~~of a method comprising~~ controlling flow of data between first and second data processing
20 systems via a memory, the step of controlling comprising:

21 by descriptor logic, generating a plurality of descriptors including a frame descriptor defining a
22 data packet to be communicated between a location in the memory and the second data
23 processing system,

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- 1 a pointer descriptor identifying the location in the memory; and
- 2 storing the descriptors generated by the descriptor logic in a descriptor table for access by the
- 3 first and second data processing systems.
- 4 21. (New) An apparatus as claimed in claim 1, wherein:
- 5 said apparatus employs Logical Communication Port architecture, and the descriptor table is
- 6 stored in one of the first data processing system and the second data processing system;
- 7 the descriptor table is stored in the second data processing system;
- 8 said apparatus employs Logical Communication Port architecture, and the descriptor logic
- 9 generates a branch descriptor comprising a link to another descriptor in the descriptor table;
- 10 the descriptor table comprises a plurality of descriptor lists sequentially linked together via
- 11 branch descriptors therein; and
- 12 the descriptor table comprises a cyclic descriptor list.

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